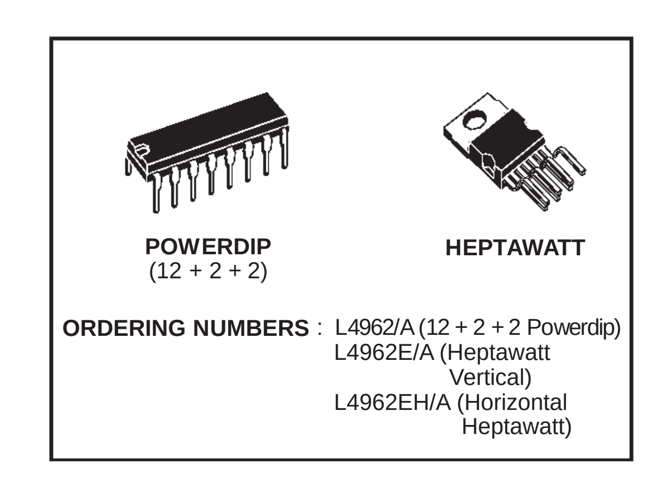


L4962

1.5A POWER SWITCHING REGULATOR

- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN



POWERDIP (12 + 2 + 2) | **HEPTAWATT**

ORDERING NUMBERS : L4962/A (12 + 2 + 2 Powerdip)
L4962E/A (Heptawatt Vertical)
L4962EH/A (Horizontal Heptawatt)

DESCRIPTION

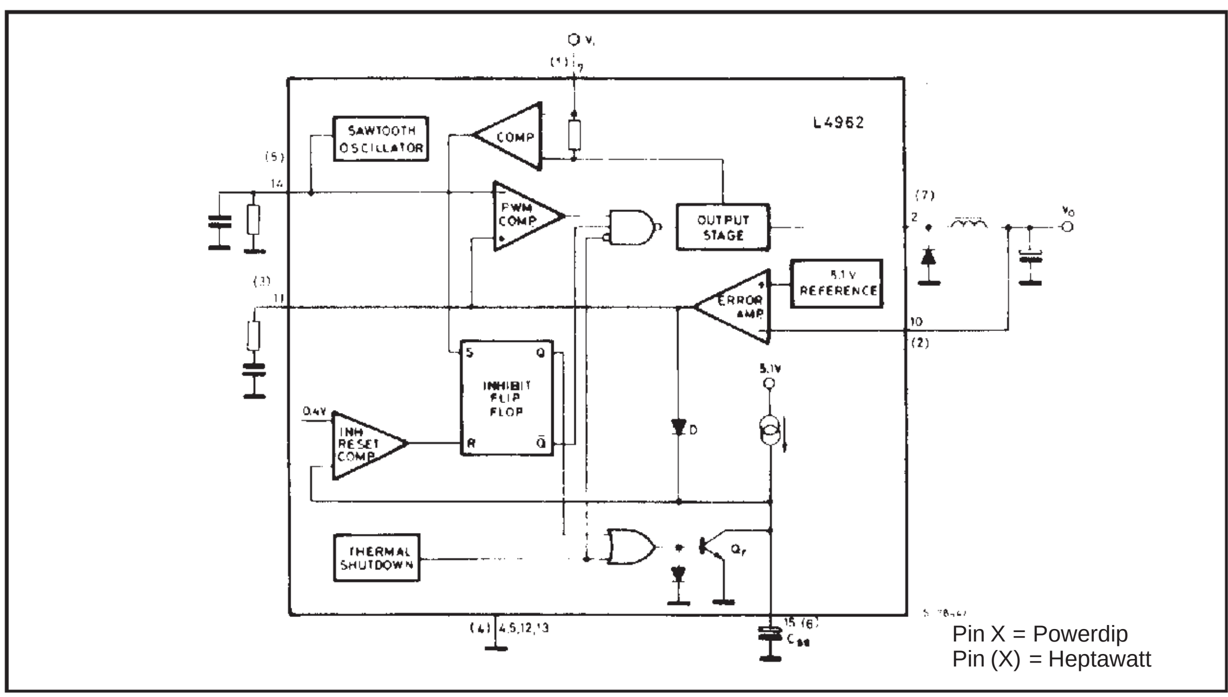
The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.

BLOCK DIAGRAM

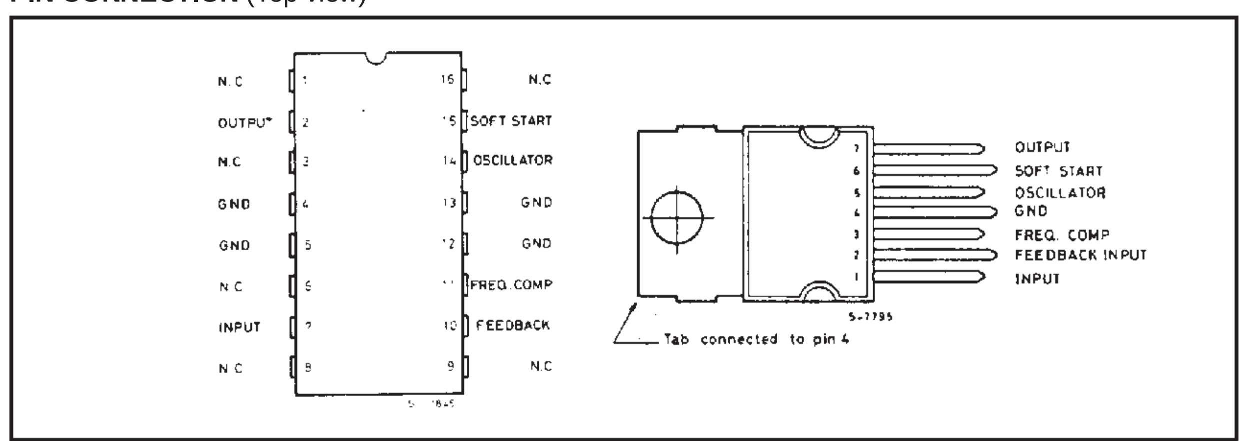


Pin X = Powerdip
Pin (X) = Heptawatt

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_7	Input voltage	50	V
V_7 - V_2	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1µs; f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leq 90°C$ (Powerdip) $T_{case} \leq 90°C$ (Heptawatt)	4.3 15	W W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	-
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	-	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.

PIN FUNCTIONS (cont'd)

HEPTAWATT	POWERDIP	NAME	FUNCTION
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25 °C, V_i = 35V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	V_o = V_{ref} to 36V	I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V V_o = V_{ref}	I_o = 1A		15	50	mV
ΔV_o	Load regulation	V_o = V_{ref}	I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A			1.5	2	V
I_{om}	Maximum operating load current	V_i = 9V to 46V V_o = V_{ref} to 36V		1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_i = 9V to 46V V_o = V_{ref} to 36V		2		3.3	A
I_{SH}	Input average current	V_i = 46V; output short-circuit			15	30	mA
η	Efficiency	f = 100KHz	V_o = V_{ref}		70		%
		I_o = 1A	V_o = 12V		80		%
SVR	Supply voltage ripple rejection	ΔV_i = $2V_{rms}$ f_{ripple} = 100Hz V_o = V_{ref}	Io = 1A	50	56		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (cont'd)							
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_i = 46V		30	40	mA
		0% duty cycle	V_i = 46V		15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle	V_i = 46V			1	mA
SOFT START							
I_{15SO}	Source current			100	140	180	µA
I_{15SI}	Sink current			50	70	120	µA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100µA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100µA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		µA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		µA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	µA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{SS} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Figure 1. Soft start waveforms

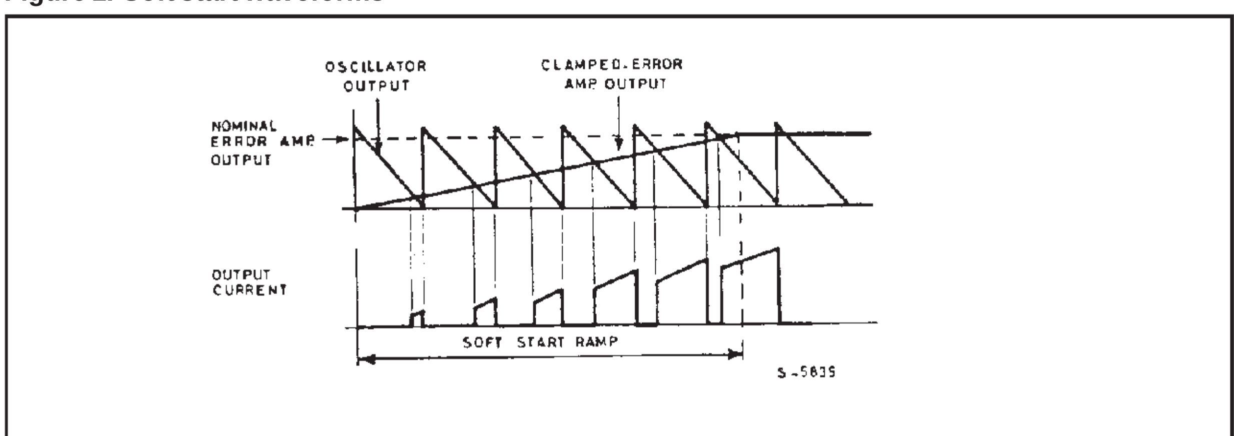


Figure 2. Current limiter waveforms

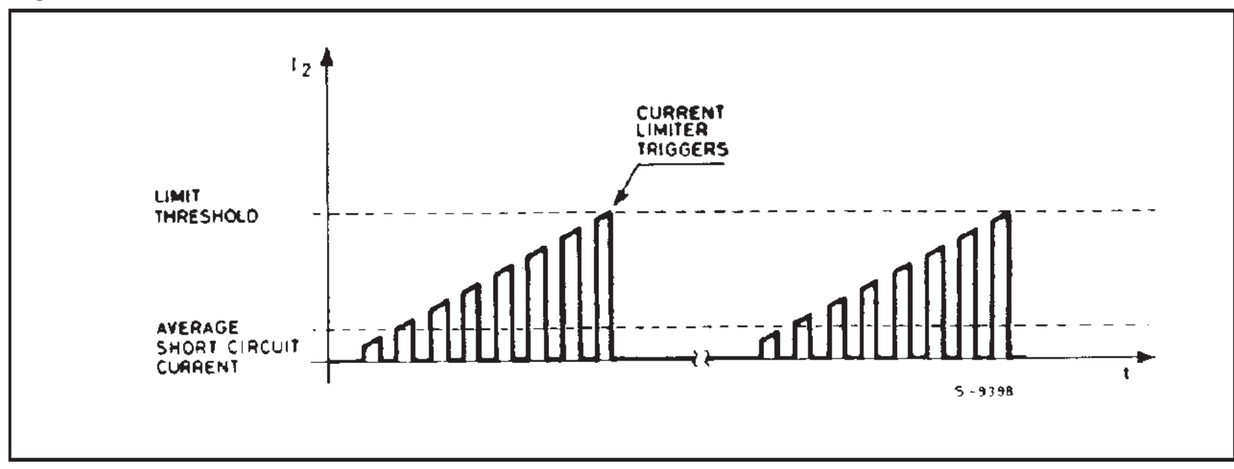
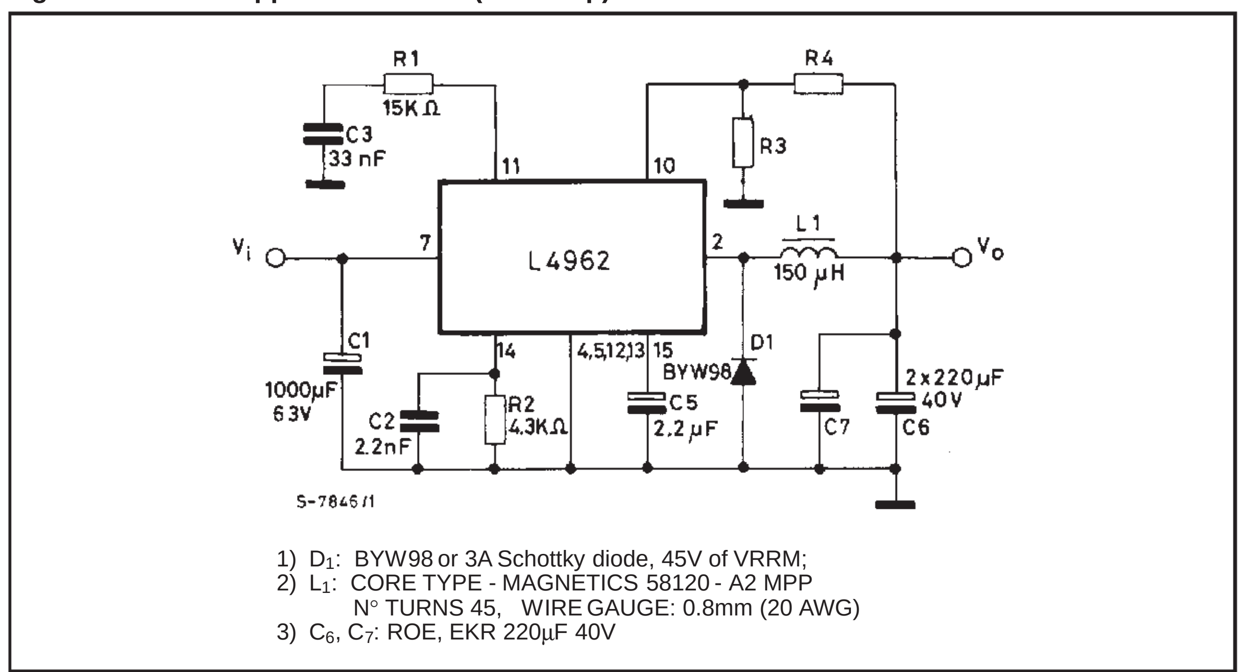


Figure 3. Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Figure 4. Quiescent drain current vs. supply voltage (0% duty cycle)

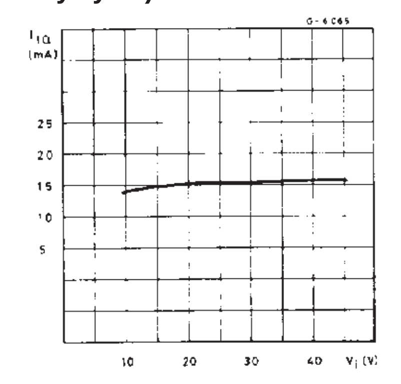


Figure 5. Quiescent drain current vs. supply voltage (100% duty cycle)

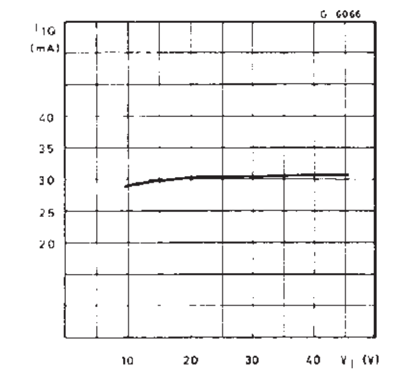


Figure 6. Quiescent drain current vs. junction temperature (0% duty cycle)

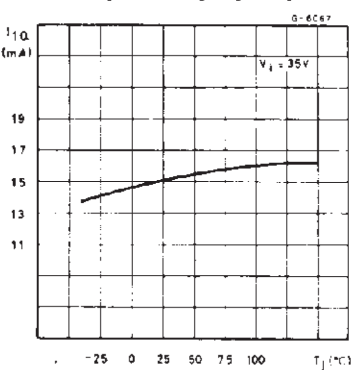


Figure 7. Quiescent drain current vs. junction temperature (100% duty cycle)

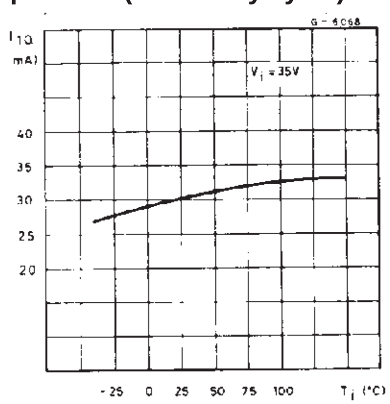


Figure 8. Reference voltage (pin 10) vs. V_i rdip) vs. V_i

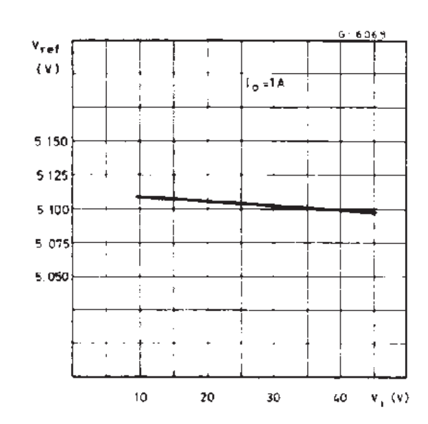


Figure 9. Reference voltage (pin 10) vs. junction temperature

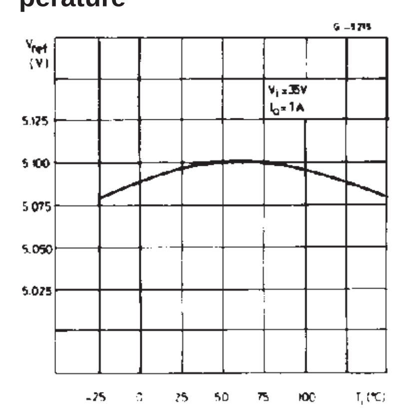


Figure 10. Open loop frequency and phase re- sponse of error amplifier

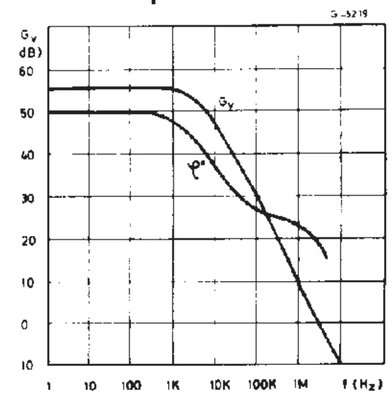


Figure 11. Switching frequency vs. input voltage

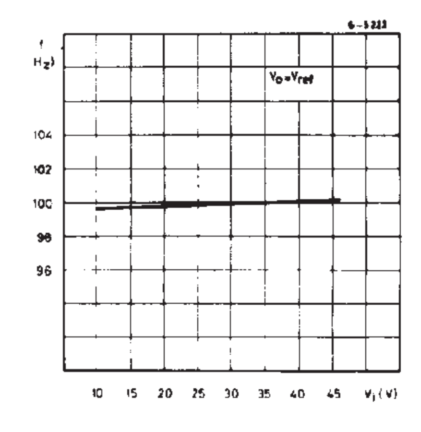


Figure 12. Switching frequency vs. junction temperature

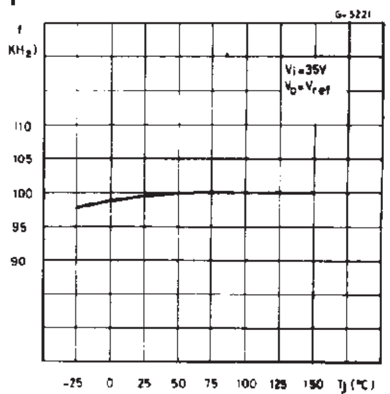


Figure 13. Switching frequency vs. R2 (see test circuit)

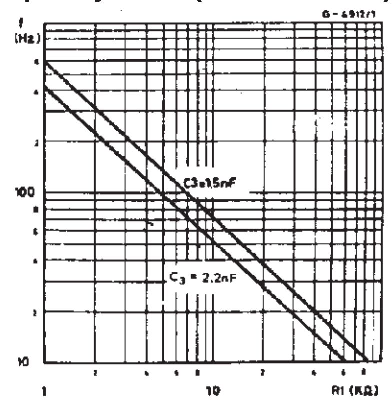


Figure 14. Line transient response

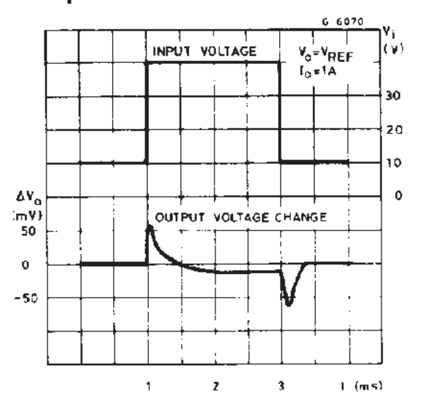


Figure 15. Load transient response

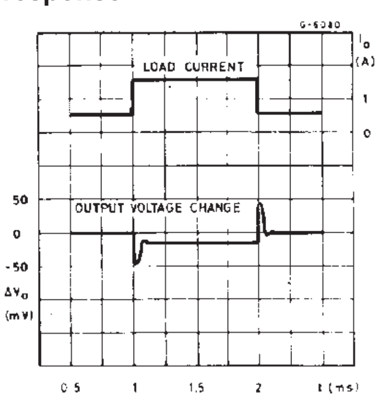


Figure 16. Supply voltage ripple rejection vs. frequency

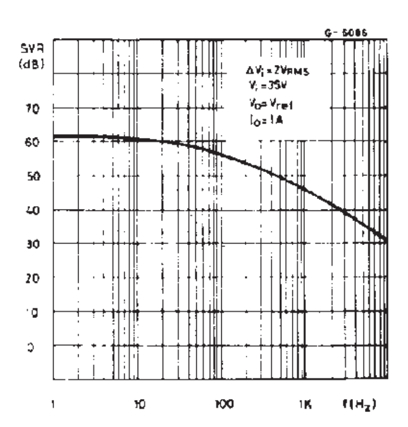


Figure 17. Dropout voltage between pin 7 and pin 2 vs. current at pin 2

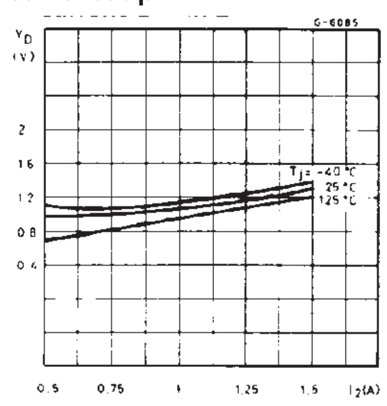


Figure 18. Dropout voltage between pin 7 and 2 vs. junction temperature

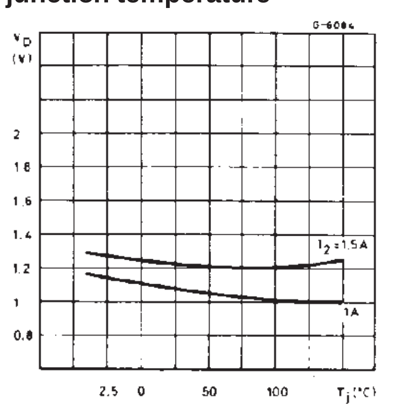


Figure 19. Efficiency vs. output current

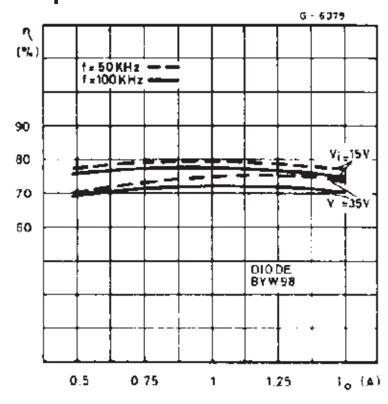


Figure 20. Efficiency vs. output current

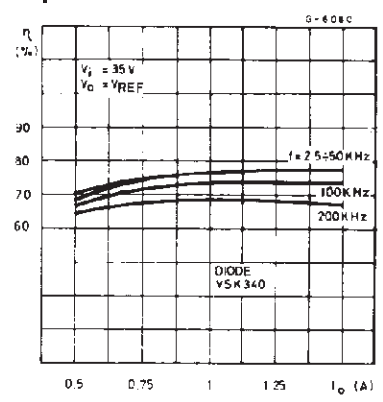


Figure 21. Efficiency vs. output current

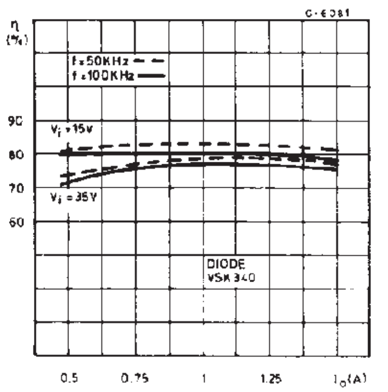


Figure 22. Efficiency vs. output voltage

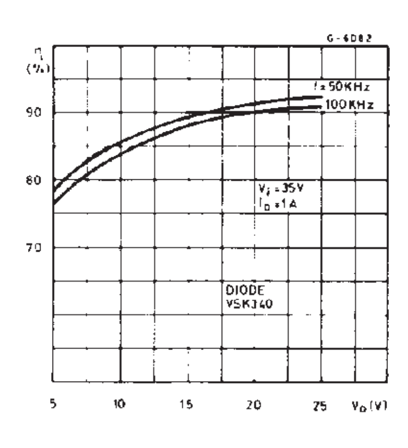


Figure 23. Efficiency vs. output voltage

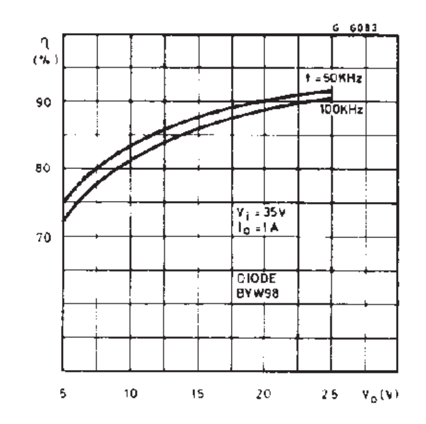
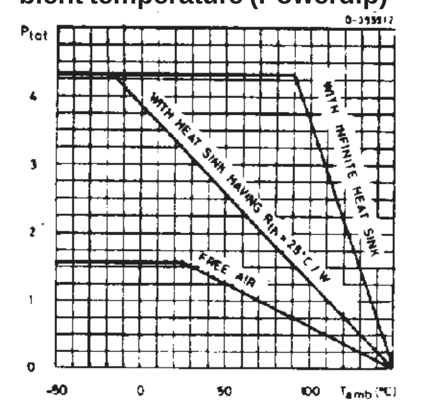
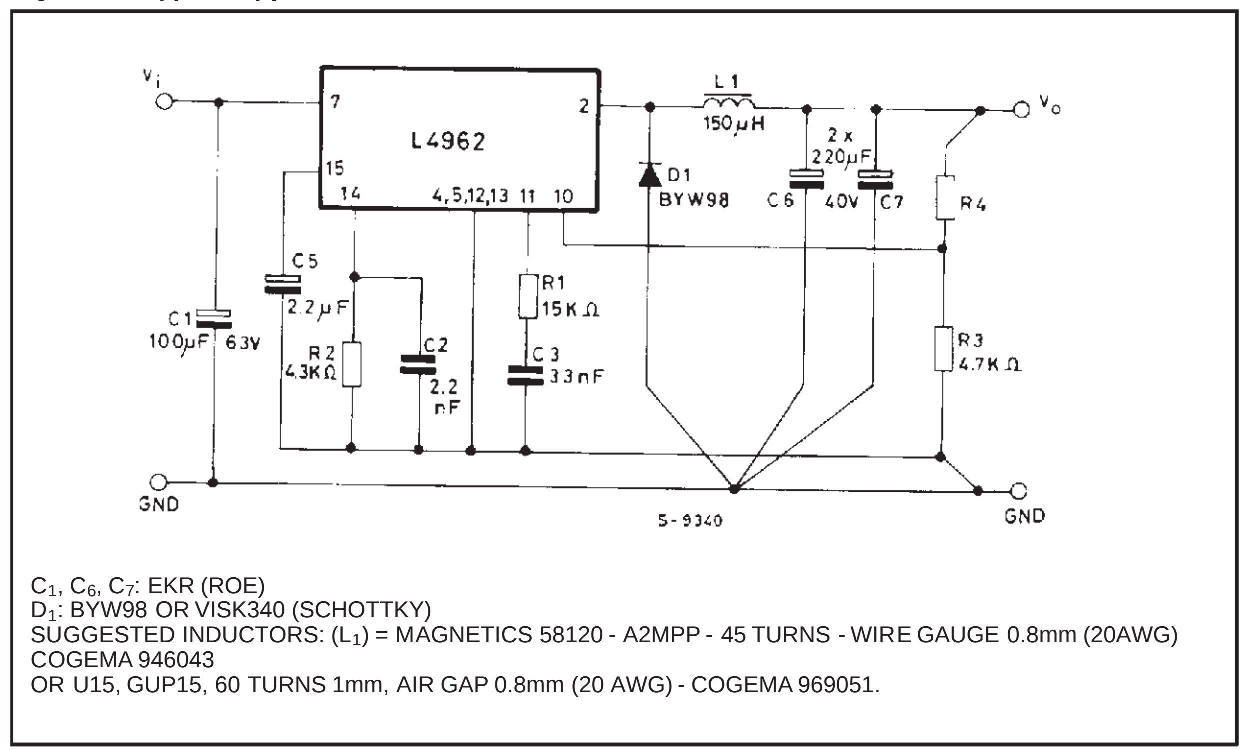


Figure 24. Maximum allowable power dissipation vs. ambient temperature (Powerdip)



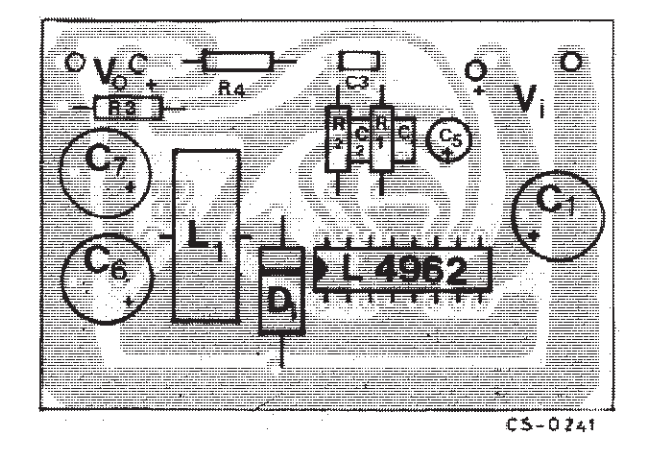
APPLICATION INFORMATION

Figure 25. Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS: (L_1) = MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20 AWG) - COGEMA 969051.

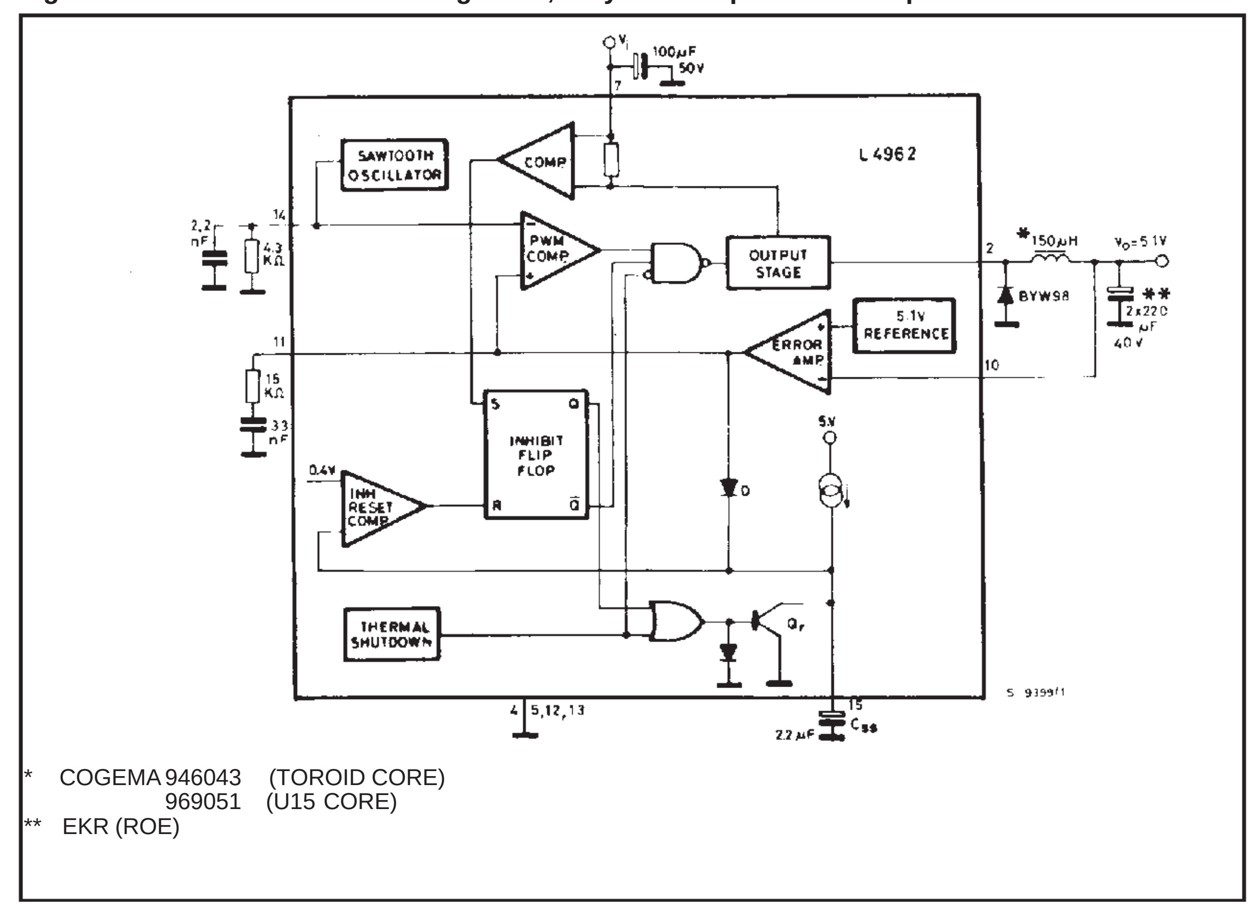
Figure 26. P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

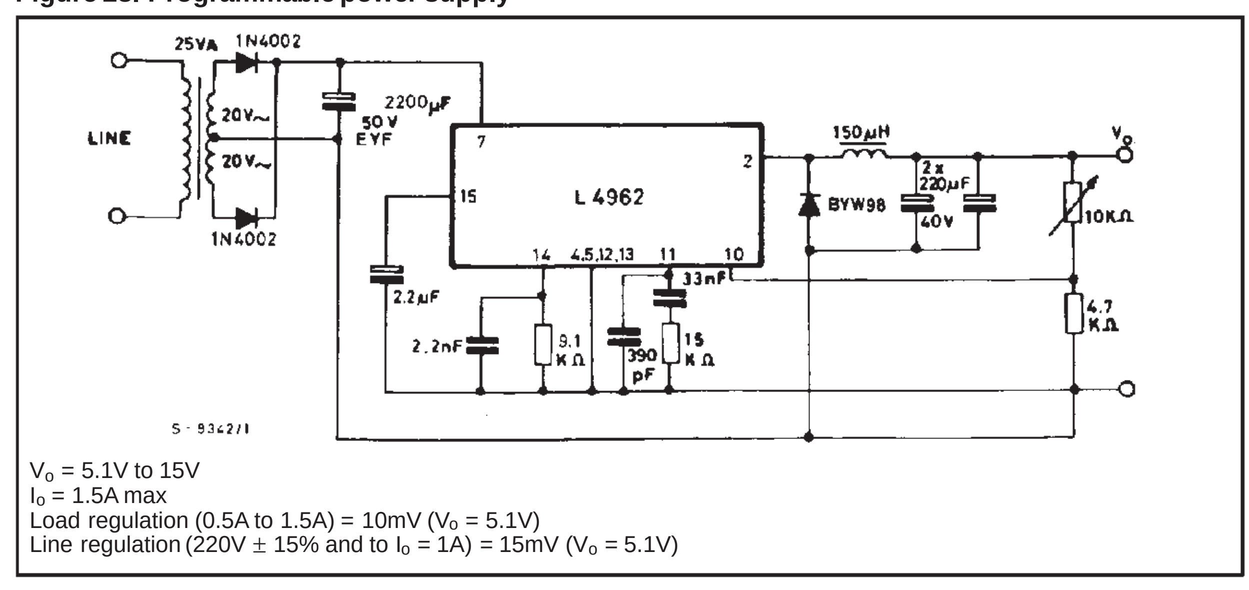
Figure 27. - A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

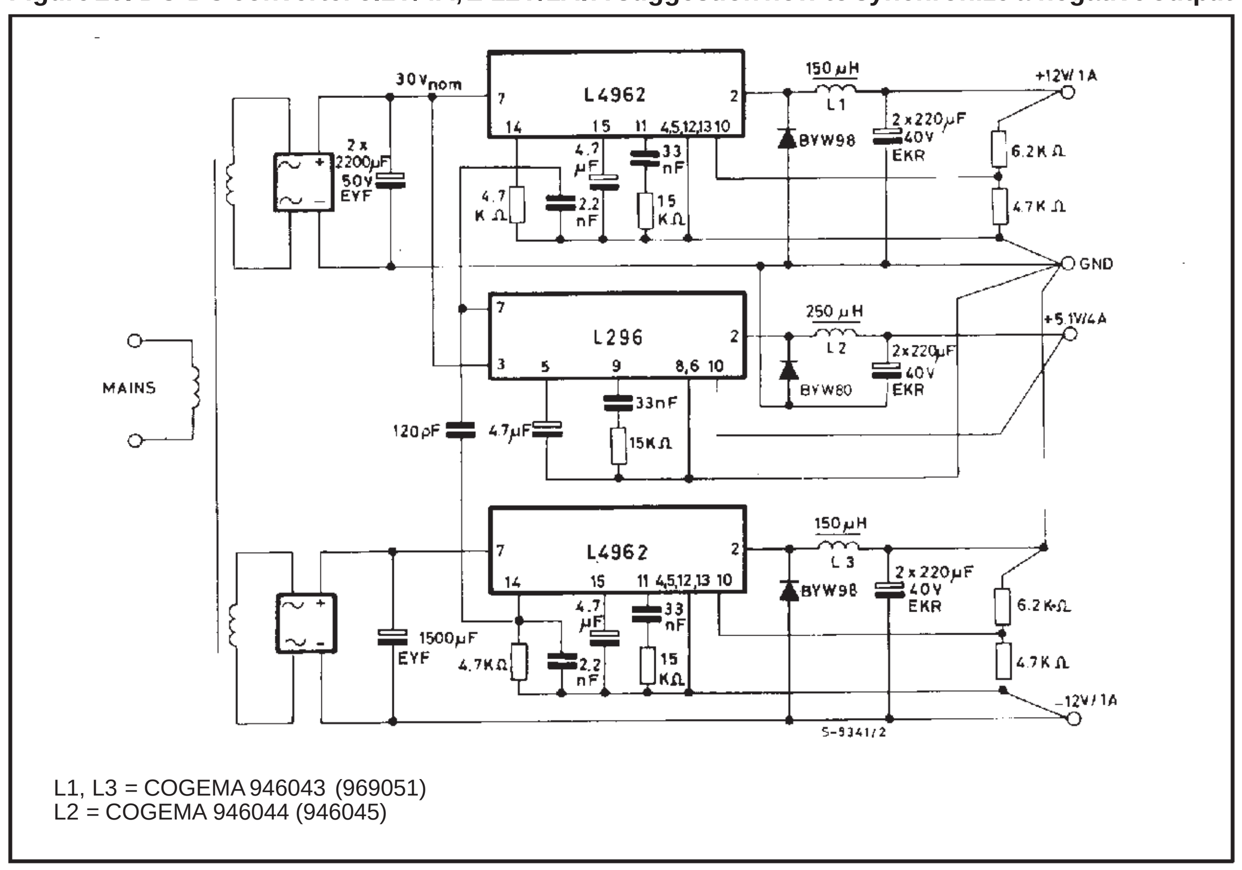
Figure 28. Programmable power supply



V_o = 5.1V to 15V
I_o = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_o = 1A) = 15mV (V_o = 5.1V)

APPLICATION INFORMATION (continued)

Figure 29. DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Figure 30. In multiple supplies several L4962s can be synchronized as shown

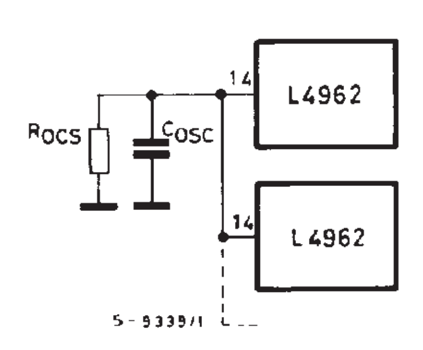
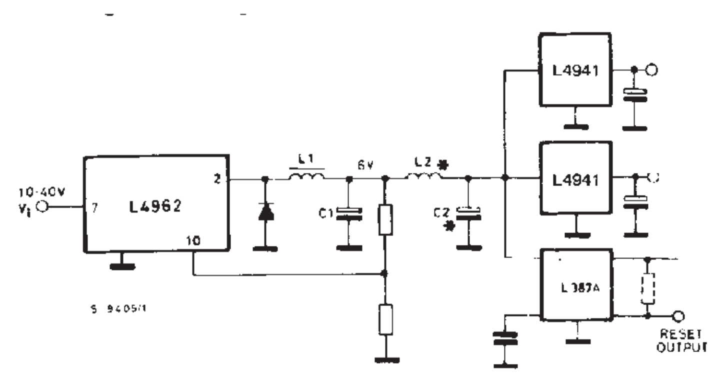


Figure 31. Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The Rth-j-amb of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).

The diagram of figure 33 shows the $R_{th\text{-}j\text{-}amb}$ as a function of the side ”l” of two equal square copper areas having the thickness of 35µ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper are must be connected to electrical ground.

Figure 32. Example of P.C. board copper area which is used as heatsink

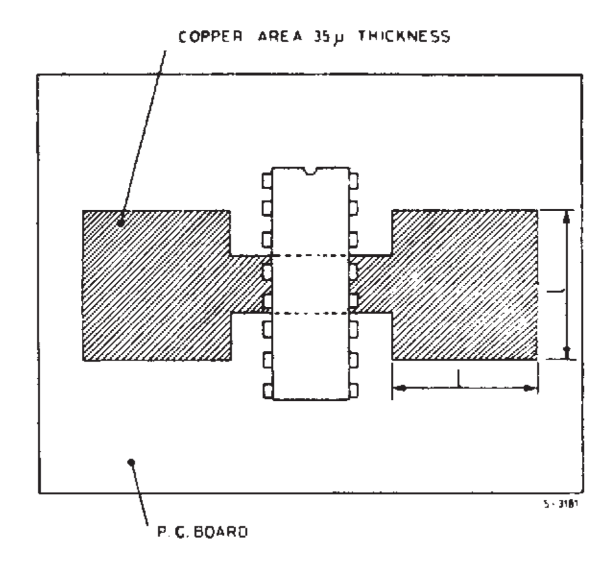
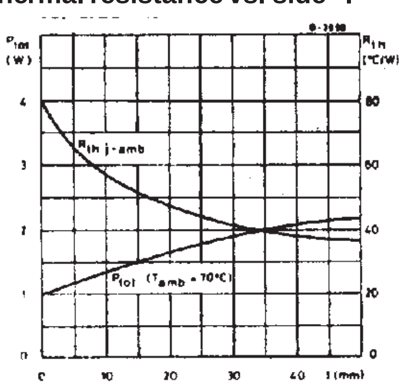
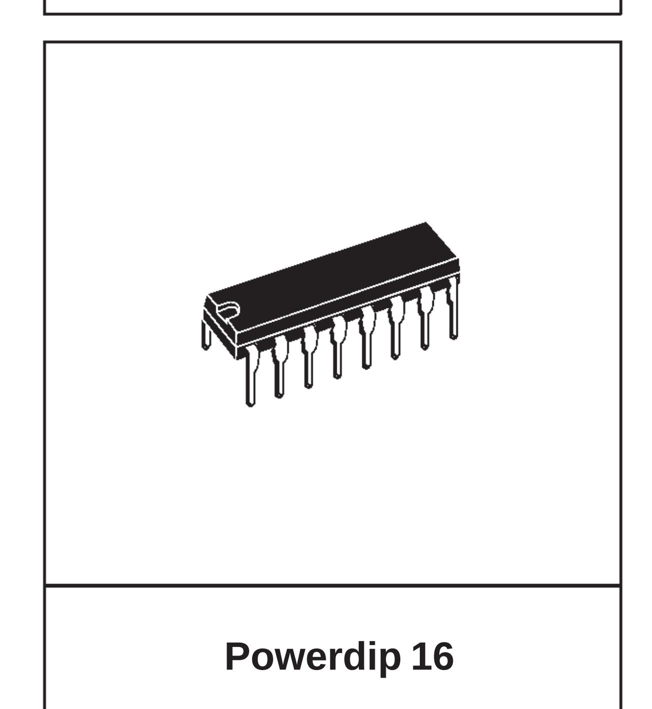


Figure 33. Maximum dissipable power and junction to ambient thermal resistance vs. side ”l”

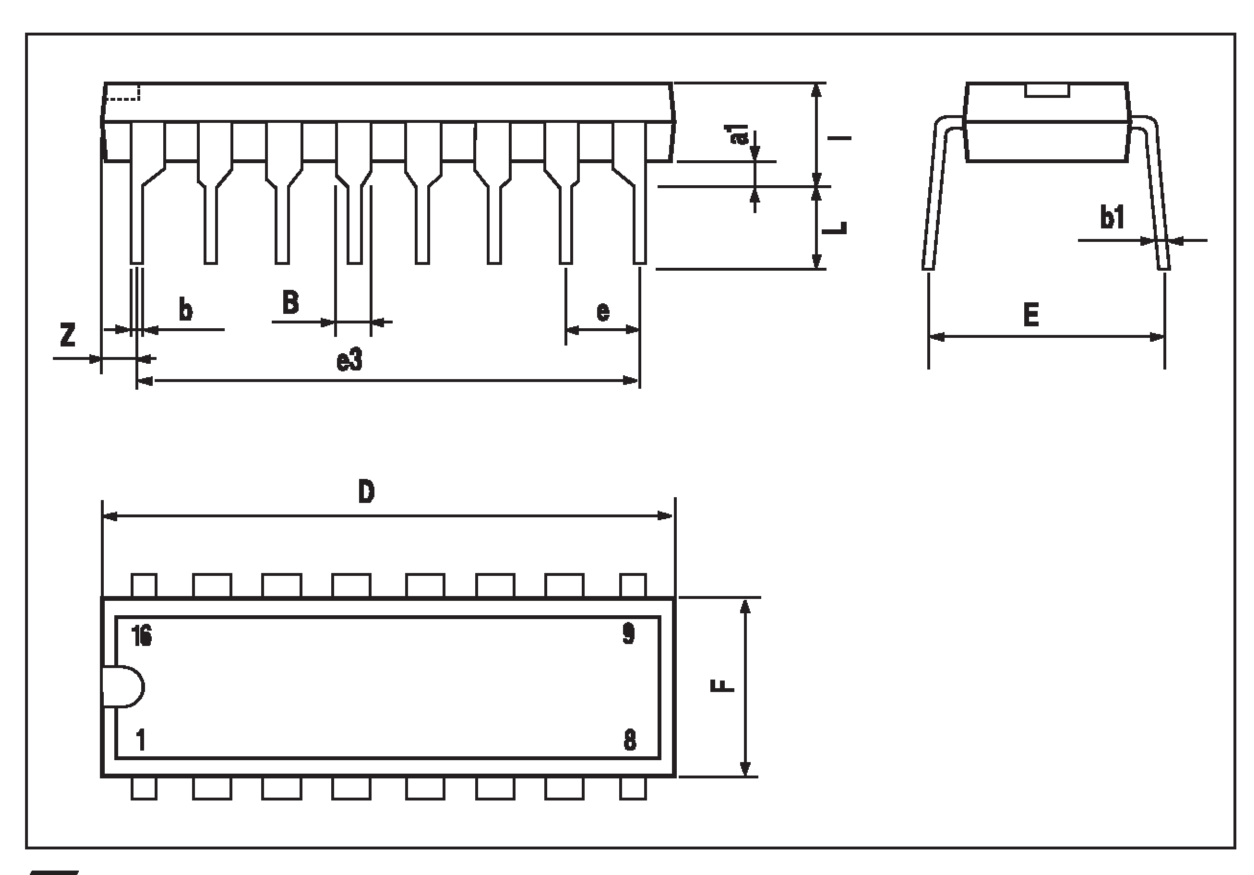


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

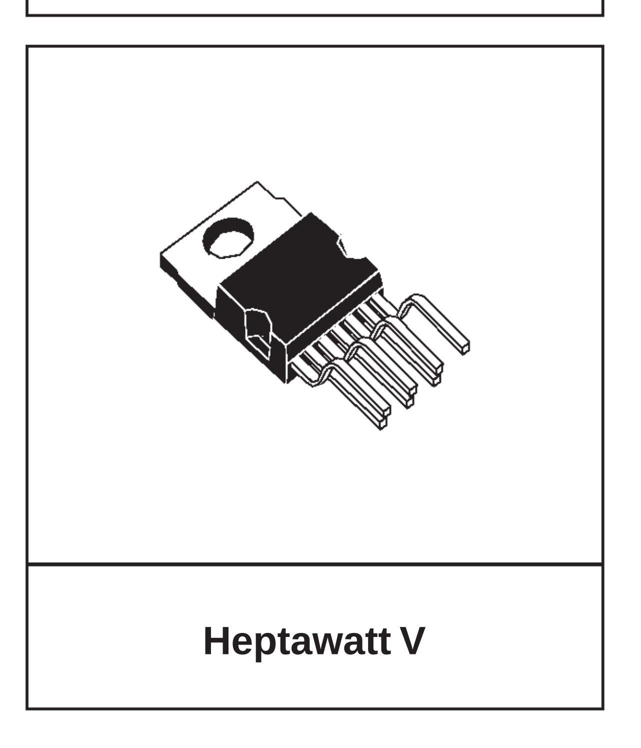


Powerdip 16

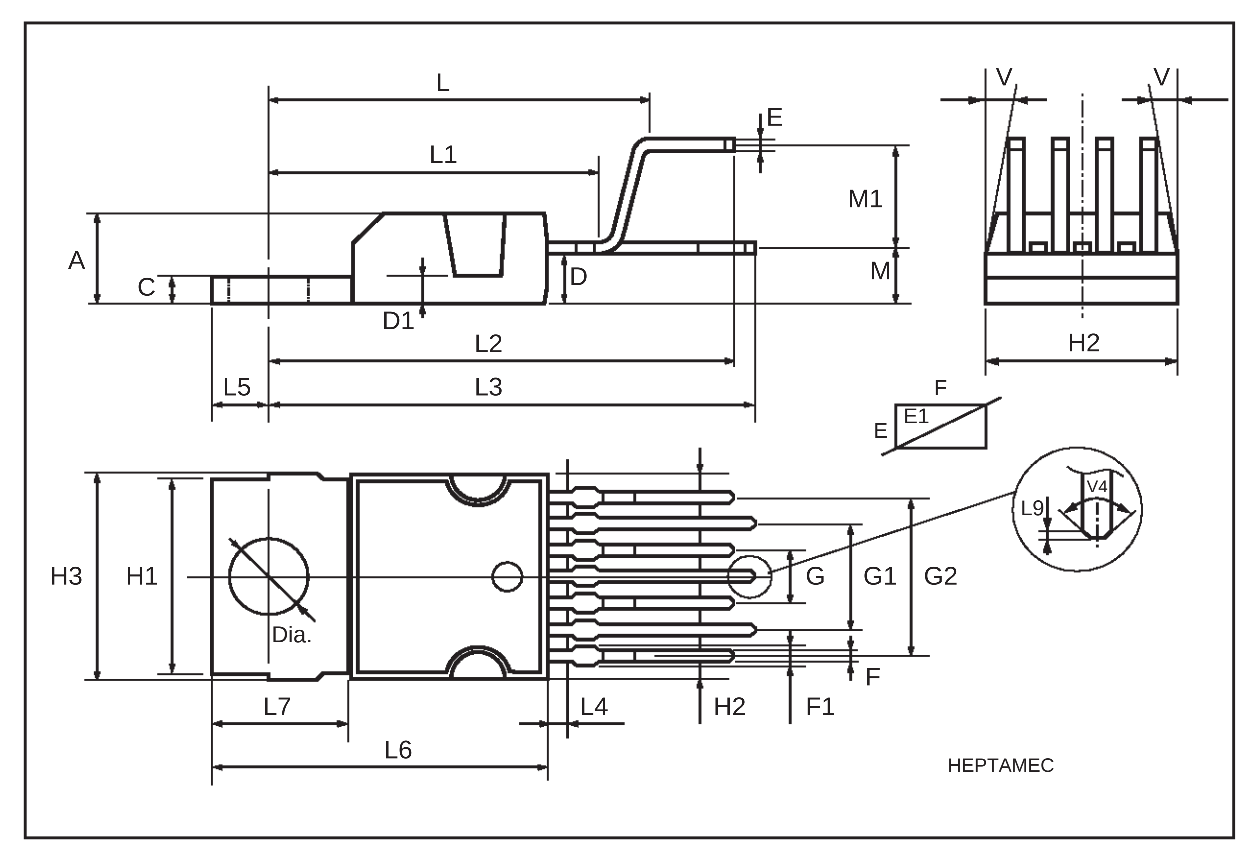


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.7		0.97	0.028		0.038
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.34	2.54	2.74	0.095	0.100	0.105
G1	4.88	5.08	5.28	0.193	0.200	0.205
G2	7.42	7.62	7.82	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L	16.7	16.9	17.1	0.657	0.668	0.673
L1		14.92			0.587	
L2	21.24	21.54	21.84	0.386	0.848	0.860
L3	22.27	22.52	22.77	0.877	0.891	0.896
L4			1.29			0.051
L5	2.6	2.8	3	0.102	0.110	0.118
L6	15.1	15.5	15.8	0.594	0.610	0.622
L7	6	6.35	6.6	0.236	0.250	0.260
L9		0.2			0.008	
M	2.55	2.8	3.05	0.100	0.110	0.120
M1	4.83	5.08	5.33	0.190	0.200	0.210
V4	40° (typ.)					
Dia	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA

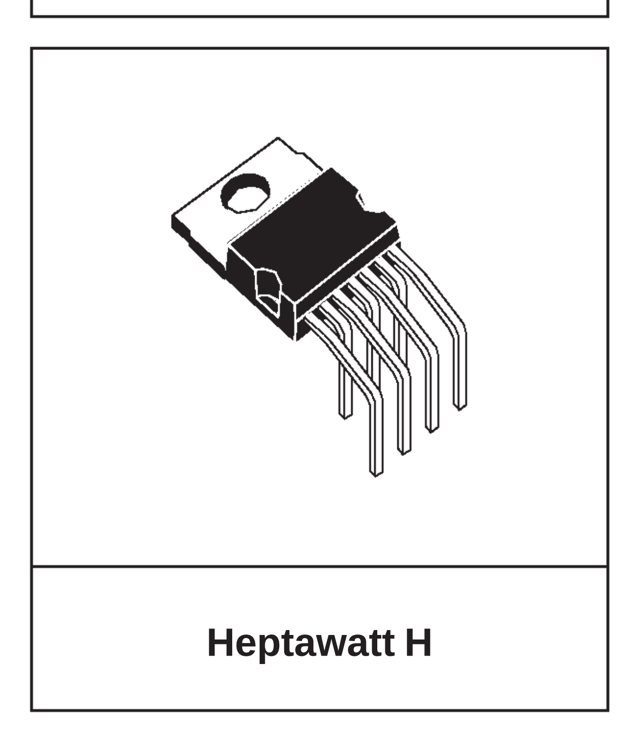


Heptawatt V



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		14.2			0.559	
L1		4.4			0.173	
L2		15.8			0.622	
L3		5.1			0.201	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
L9		4.44			0.175	
Dia	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Heptawatt H

